In the claims:

1. (Cancelled)

2. (Currently Amended) Method according to claim ~~1~~3, ~~characterised in that~~wherein it is applied to cells having a higher threshold than the original one.

3. (Currently Amended) A single cell erasing method for recovering memory cells under reading or programming disturbs, in non volatile semiconductor memory electronic devices comprising cell matrix split in sectors and organized in rows, or word line, and columns, or bit lines, of the type providing the application of a sector erasing algorithm with subsequent testing phase (erase-verify), wherein it provides a bit by bit erasing by applying to each single word line a negative voltage used during the erasing of a whole sector and on the drain terminal of each single cell a programming voltage, the method further providing ~~Method according to claim 1, characterised in that it provides also~~ a bias to a negative voltage value of the cell substrate or of the cell bulk terminal to increase a drain junction bias and enhance impact ionization at a drain junction in order to accelerate the generation of hot holes to be injected into a floating gate.

4. (Currently Amended) Method according to claim ~~1~~3, ~~characterised in that~~wherein it provides initially a search phase of which cells have a higher threshold voltage than the original value and a subsequent application phase of said bit by bit erasing.

5. (Currently Amended) Method according to claim ~~1~~3, ~~characterised in that~~wherein a subsequent erase-verify phase is performed after the bit by bit erasing.

6. (Currently Amended) Method according to claim ~~1~~3, ~~characterised in that~~wherein said cell matrix is a Page-Flash array.

7-13. (cancelled)

14. (Currently Amended) The flash memory device of claim ~~13~~ 15 wherein the memory-cell array comprises a page-flash array.

15. (Currently Amended) A flash memory device including a memory-cell array, the memory cell array being arranged in sectors with each sector including a portion of the memory cells contained in the array, each flash memory cell in the array having a control terminal coupled to a word line and a drain terminal coupled to a bit line, the memory device being operable to erase selected memory cells in a sector by applying a negative programming voltage on a selected word line of the sector and applying a positive voltage on a selected bit line of the sector of memory cells, and ~~The flash memory device of claim 13~~ wherein the memory device is further operable to determine which memory cells in the sector have a threshold voltage greater than a threshold value and to apply the negative programming voltage and positive voltage to all memory cells in the sector determined to have threshold voltages greater than the threshold value, and wherein the memory device is further operable to bias at a negative voltage value a cell substrate or of the cell bulk terminal to increase a drain junction bias and enhance impact ionization at a drain junction in order to accelerate the generation of hot holes to be injected into a floating gate.

16. (Original) The flash memory device of claim 15 wherein the memory device is further operable to apply to each memory cell determined to have a threshold voltage greater than the threshold value a test voltage having a value equal to an erase-verify voltage plus a voltage margin.

17. (Currently Amended) An electronic system, comprising:

a flash memory device, including,

a memory-cell array, the memory cell array being arranged in sectors with each sector including a portion of the memory cells contained in the array, each flash memory cell in the array having a control terminal coupled to a word line and a drain terminal coupled to a bit line, the memory device being

operable to erase selected memory cells in a sector by applying a negative programming voltage on a selected word line of the sector and applying a positive voltage on a selected bit line of the sector of memory cells, wherein the memory device is further operable to determine which memory cells in the sector have a threshold voltage greater than a threshold value and to apply the negative programming voltage and positive voltage to all memory cells in the sector determined to have threshold voltages greater than the threshold value, and wherein the memory device is further operable to bias at a negative voltage value a cell substrate or of the cell bulk terminal to increase a drain junction bias and enhance impact ionization at a drain junction in order to accelerate the generation of hot holes to be injected into a floating gate.

18. (Original) The electronic system of claim 17 wherein the system comprises a computer system.

19. (Original) The electronic system of claim 17 wherein the memory-cell array comprises a page-flash array.

20. (Original) The electronic system of claim 17 wherein the memory device is further operable to determine which memory cells in the sector have a threshold voltage greater than a threshold value and to apply the negative programming voltage and positive voltage to all memory cells in the sector determined to have threshold voltages greater than the threshold value.